BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

Fig. 1 illustrates a block diagram of a system incorporating a place and route tool with enhanced control over the layout of structured elements;

Fig. 2 illustrates a flow chart describing the operation of the system of Fig. 1;

Fig. 3a illustrates a matrix used to define the layout of cells in the place and route tool;

Fig. 3b illustrates spacing between matrix rows;

Fig. 3c illustrates the use of spacing between rows to achieve interleaved matrices; and

Fig. 4 illustrates space left in structured layout matrices used for unstructured cells.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is best understood in relation to Figures 1-4 of the drawings, like numerals being used for like elements of the various drawings.

Figure 1 illustrates a block diagram showing the overall structure of a system 10 for placing and routing cell in a complex circuit that provides full control on the placement of highly critical structured logic. A place and route tool 12, receives information from a datapath generator 14 that defines the desired layout for the structured logic (also referred to herein as the "datapath" cells) in a language configuration file compatible with the place and route tool. Information for the remainder of the cells (also referred to herein as the "control" or "unstructured" cells) is input from input source 16, which could be a file or input device. The datapath generator 14 and place and route tool 12 may be implemented on the same or separate workstations or similar computing devices.

Figure 2 is a flowchart describing the basic operation of the system 10 of Figure 1. In block 18, the cell information for the circuit is entered into the place and route tool 12. In block 20, the datapath generator 12, which is a program that generates a file describing the desired layout information for the datapath cells, generates a configuration file. This configuration file defines the layout of the datapath cells of the circuit. The datapath generator 14 allows the layout designer to have complete control of the placement of these cells. This aspect is described in greater detail hereinbelow.

In block 22, the datapath logic layout is "fixed" in the place and route tool 12. In the AVANT! APOLLO product, cells may be fixed through assignment of a "fixed" status to the cells, which provides the highest layout priority; the

placement location of these cells is guaranteed as other cells are moved to optimize timing performance.

In step 24, timing (or other) constraints for the remaining unstructured cells (the "control logic") are submitted to the place and route tool 12. The place and route tool 12 can optimize the layout in step 26, without affecting the previously-fixed placement of the datapath logic. When timing (or other) constraints are met, the layout information can be generated in block 28.

The present invention as described in Figures 1 and 2 provides the layout designer with the ability to carefully and flexibly place critical structured logic in a desired arrangement, which will not be affected by subsequent optimization routines by the place and route tool 12.

Figures 3a-c illustrate the placement of the structured logic in greater detail. The illustrated embodiment uses the operation of the AVANT! APOLLO place and route tool as an example of how the structured datapath logic can be allocated in a place and route tool; other products may use different methods of allocating cells in a matrix.

Figure 3a illustrates an empty matrix 30. A cell matrix is defined, at a minimum, by a unique name, a number of rows 34 and a number of columns 36. Each slot 32 of an empty matrix is initially square, i.e., the height and width of each slot 32 is the height of the unit tile cell. Each slot 32 is assigned a row and column number. Once a cell is assigned to a slot 32, the corresponding matrix column 36 is enlarged according to the cell width of the slot 32.

Column and row space can be adjusted by adding extra space between rows 34 or between columns 36. In Figure 3b, extra space 38 is added between rows 34. This feature can be used to allow two or more matrices to be